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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/681,643	05/15/2001	Takatoshi Tsujimura	JP920000112US1	8744

35060 7590 03/20/2007

THE LAW OFFICE OF IDO TUCHMAN
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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/681,643	TSUJIMURA ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,17-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,17-20,22 and 23* is/are rejected.

7)☒ Claim(s) *24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 18, 2007 has been entered.

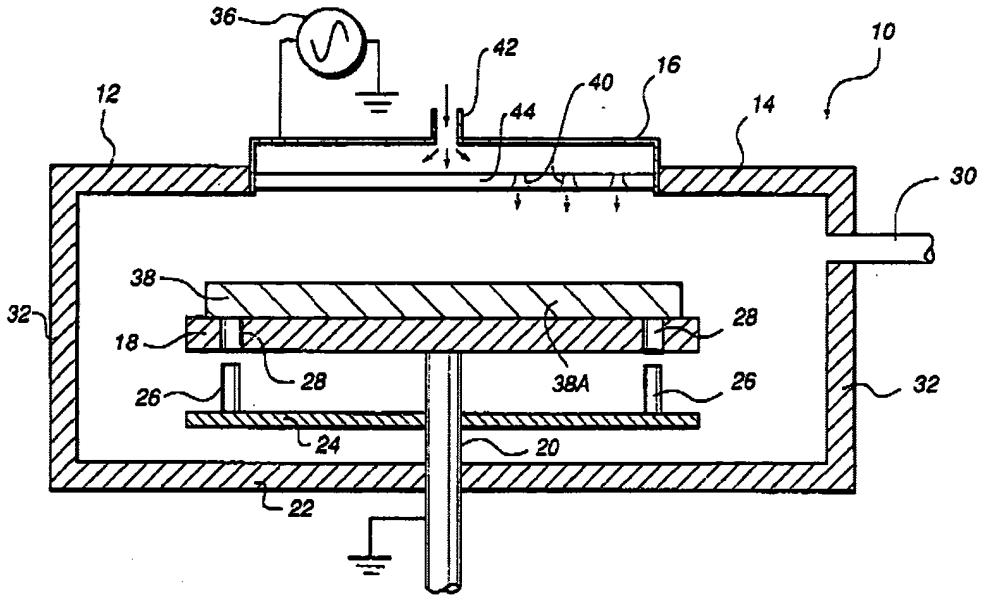
Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 6-8, 17-20 and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Law et al., U.S. Patent 5,589,233.

4. Law discloses a semiconductor process as claimed. See **FIGS. 1-2** where Law teaches the following limitations.



5. Pertaining to claim 1, Law teaches a manufacturing method of an active matrix device including a top gate TFT (please note that Law teaches at least two (2) major types of transistor devices, it is inherent that one is a top gate TFT, see column 1, lines 65-68), which comprises a process of forming the top gate TFT, wherein the process of forming the top gate type TFT includes the steps of:

forming an oxide film specifically on a substantially entire inner wall of a CVD processing chamber (Law teaches there is sufficient residual insulating material to substantially cover the chamber walls, see column 3, lines 9-15);

arranging a substrate having source and drain electrodes formed therein in the processing chamber (please note that the Examiner takes the position that all active matrix TFT's have source and drain electrodes);

doping the source and drain electrodes with P (please note that the Examiner takes the position that P in the present claim is referring to phosphorus, column 2, line 4);

forming an a-Si layer and a gate insulating film in the CVD processing chamber, wherein the step of doping the source and drain electrodes with P and the step of forming the a-Si layer and the gate insulating film are carried out in-situ in the CVD processing chamber; and

wherein forming the oxide film specifically on the substantially entire inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P.

6. Pertaining to claim 2, Law teaches a manufacturing method of an active matrix device according to claim 1, wherein the process of forming the top gate type TFT further comprises the step of removing the oxide film from the substantially entire inner wall after the step of forming the a-Si layer and the gate insulating film (see column 5, line 63).

7. Pertaining to claim 3, Law teaches a manufacturing method of an active matrix device according to claim 1, wherein the oxide film contains SiOx (see column 5, line 4, also note that the term silicon oxide includes monoxides as well as dioxide materials).

8. Pertaining to claim 4, Law teaches a manufacturing method of an active matrix device according to claim 1, wherein the active matrix device is a liquid crystal display (see column 1, line 43).

9. Pertaining to claim 6, Law teaches a manufacturing method of an active matrix device according to claim 2, wherein the oxide contains an SiOx.

10. Pertaining to claim 7, Law teaches a manufacturing method of an active matrix device according to claim 2, wherein the active matrix device is a liquid crystal display.
Pertaining to claim 8, Law teaches a manufacturing method of an active matrix device according to claim 2, wherein the active matrix device is a liquid crystal display.

11. Pertaining to claim 17, Law teaches a manufacturing method of an active matrix device according to claim 1, further comprising heating substantially entire wall of the CVD processing chamber so as to facilitate forming the oxide film specifically on the substantially entire inner wall of the CVD processing chamber (it is an inherent fact that heating is required to form a gate oxide for a TFT).

12. Pertaining to claim 18, Law teaches a method of an active matrix device according to claim 1, wherein the oxide film is selected from SiOx.

13. Pertaining to claim 19, Law teaches a manufacturing method of an active matrix device including a top gate type TFT, which comprises a process of forming the top gate type TFT, wherein the process of forming the top gate type TFT includes the steps of:

forming an oxide film specifically on a substantially entire inner wall of a CVD processing chamber, the oxide film being at least 50 nm thick (see column 5, lines 1-3);
arranging a substrate having source and drain electrodes formed therein in the CVD processing chamber;

doping the source and drain electrodes with P;

forming an a-Si layer and a gate insulating film in the CVD processing chamber, wherein the step of doping the source and drain electrodes with P and the step of forming the a-Si layer and the gate insulating film are carried out in-situ in the CVD processing chamber; and

wherein forming the oxide film on the substantially entire inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P.

14. Pertaining to claim 20, Law teaches a manufacturing method of an active matrix device according to claim 19, wherein the oxide film is approximately 100 nm (please see column 5, lines 1-3).

15. Pertaining to claim 22, Law teaches a manufacturing method of an active matrix device according to claim 1, further comprising:

depositing a first gate insulating film;

forming the first gate insulating film before forming the oxide film on the substantially entire inner wall of the CVD processing chamber;

depositing a second gate insulating film after forming the a-Si layer;

removing the oxide film after depositing the second gate insulating film;

wherein forming the oxide film on the substantially entire inner wall of the CVD processing chamber is performed before doping the source and drain electrodes with P; and

wherein the step of doping the source and drain electrodes with P, the step of forming the a-Si layer, and the step of depositing the second gate insulating film are carried out in-situ in the CVD processing chamber (because Law uses an single chamber, this limitation has been met).

Pertaining to claim 23, Law teaches a manufacturing method of an active matrix device according to claim 19, wherein the oxide film contains SiOx.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 5, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Law et al., U.S. Patent 5,589,233 in view of Ohnuma et al., U.S. Patent 6,072,193.

18. Pertaining to claims 5, 9 and 10, Law fails to teach a manufacturing method wherein the active matrix device is an electroluminescence display. Ohnuma teaches wherein the active matrix device is an electroluminescence display (see column 17, line 62). In view of Ohnuma, it would have been obvious to one of ordinary skill in the art to incorporate an electroluminescence display into the Law semiconductor manufacturing method because an EL display can be used for capturing information (see column 17, line 65).

Objections

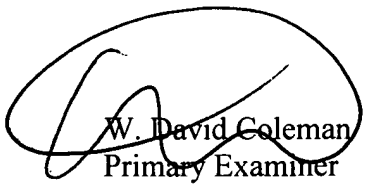
19. Claim 24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



W. David Coleman
Primary Examiner
Art Unit 2823

WDC